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DATE MAILED: 06/04/2003

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
09/925,214	08/08/2001	Ted Moise	10003787-1	3138
7	590 06/04/2003			
AGILENT TECHNOLOGIES, INC.			EXAMINER	
Legal Department, DL429 Intellectual Property Administration			DICKEY, THOMAS L	
P.O. Box 7599 Loyeland, CO 80537-0599			ART UNIT	PAPER NUMBER
Loveland, CO	80337-0377		2826	

Please find below and/or attached an Office communication concerning this application or proceeding.

	1 A . 12 - 4: N1 -		
	Application No.	Applicant(s)	
Office Astion Communication	09/925,214	MOISE ET AL.	
Office Action Summary	Examiner	Art Unit	
	Thomas L Dickey	2826	
The MAILING DATE of this communication app Period for Reply	pears on the cover	sheet with the correspondence ad	ldress
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.1: after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply If NO period for reply is specified above, the maximum statutory period v - Failure to reply within the set or extended period for reply will, by statute - Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	36(a) In no event, howev y within the statutory minin vill apply and will expire S , cause the application to	er may a reply be timely filed num of thirty (30) days will be considered timel IX (6) MONTHS from the mailing date of this c become ABANDONED (35 U S C § 133)	
Status	1 m mil 2002		
1) Responsive to communication(s) filed on 14 A		-1	
·—	is action is non-fin		
 Since this application is in condition for allowards closed in accordance with the practice under Disposition of Claims 			ie ments is
4) Claim(s) <u>39-41 and 57-59</u> is/are pending in the	e application.		
4a) Of the above claim(s) is/are withdraw	wn from considera	tion.	
5) Claim(s) is/are allowed.			
6) Claim(s) <u>39,40,57 and 58</u> is/are rejected.			
7) Claim(s) <u>41 and 59</u> is/are objected to.			
8) Claim(s) are subject to restriction and/o	r election requirem	ient.	
Application Papers			
9) The specification is objected to by the Examine	r.		
10)∑ The drawing(s) filed on <u>08 August 2001</u> is/are:		·	
Applicant may not request that any objection to the			
		d b) disapproved by the Examin	er.
If approved, corrected drawings are required in rep	•	on.	
12) The oath or declaration is objected to by the Ex	ammer.		
Priority under 35 U.S.C. §§ 119 and 120		11.0.0.0.140(a) (d) or (f)	
13) Acknowledgment is made of a claim for foreign	i priority under 35	0.5.C. § 119(a)-(a) or (i).	
a) All b) Some * c) None of:	- hava basa rasai	vo d	
1. Certified copies of the priority documents			
2. Certified copies of the priority documents			Stago
3. Copies of the certified copies of the prior application from the International Bu * See the attached detailed Office action for a list	reau (PCT Rule 17	7.2(a)).	Stage
14) Acknowledgment is made of a claim for domestic	c priority under 35	U.S.C. § 119(e) (to a provisional	l application).
a) The translation of the foreign language pro15) Acknowledgment is made of a claim for domesting			
Attachment(s)			
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)	5) 🔲 1	nterview Summary (PTO-413) Paper No Notice of Informal Patent Application (PT Other	
S. Patent and Trademark Office			

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DETAILED ACTION

1. The amendment filed on 04/16/03 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b) by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 39,40,57, and 58 are rejected under 35 U.S.C. 102(e) as being anticipated by KIMURA et al. (2002/0192901).

With regard to claim 39-40, the first embodiment of Kimura et al. discloses an integrated circuit comprising:

- 1. a transistor level 6 and an overlying transistor isolation layer 8,
- 2 a ferroelectric structure, positioned over the transistor isolation layer ε. including
- 3 a ferroelectric device level 14 disposed over the transistor isolation layer 8.
- 4 [an] overlying ferroelectric isolation layer 16,
- 5 a first metal layer 21,

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- 6. an inter-level dielectric level 22 disposed over the first metal layer 21; and
- 7. a second metal layer 23 disposed over the inter-level dielectric level 22.

With regard to claim 57-58, the first embodiment of Kimura et al. discloses a method of forming an integrated circuit, comprising the steps of:

- 1. forming a transistor level 6 and an overlying transistor isolation layer 8
- 2. forming a ferroelectric device level 14 over the transistor isolation layer 8,
- 3. forming a first metal layer 21 over the ferroelectric device level 14;
- 4. forming an inter-level dielectric level 22 over the first metal layer 21:
- forming a second metal layer 23 disposed over the inter-level dielectric level
 and
- 6. [an] overlying ferroelectric isolation layer 16,

With regard to both of all of claims 39,40, 57, and 58, the first embodiment of Kimura et al. discloses that the transistor level 6 comprises one or more semiconductor devices 2-3-4-5 disposed over a substrate 1, the overlying transistor isolation layer 8 has at least one contact via (9' or 13) extending therethrough, the ferroelectric device level 14 includes at least one ferroelectric capacitor 19-20, the overlying ferroelectric isolation layer 16 has at least one via (no number, it is immediately left of via 17 in figure 1, and is formed at the same time as via 17, see figure 11) extending there through, and the via is laterally sized larger than a corresponding contact via (9') aligned therewith.

Furthermore, with regard to claims 40 and 58, contact vias 9', formed in overlying transistor isolation layer 8, may be filled with tungsten contact plugs. Note that Kimura

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et al. only discloses tungsten plugs with regard to contact vias 9', and that according to Kimura et al. contact vias 13 are formed from polysilicon.

Note figures 1 and 3-16 and paragraphs 0136-0161 of Kimura et al.

Allowable Subject Matter

3. Claims 41 and 59 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 41 and 59 would be allowed over the references of record for the following reasons:

As explained above with reference to claims 40 and 58, Kimura et al. discloses all aspects of claims 41 and 59 except that the tungsten plugs formed under the ferroelectric capacitors. However, in paragraph 0039 Kimura et al. states that:

[A]ccording to the present invention, as shown in FIG. 1, the trench is formed through not a thick dielectric film but stacked plural dielectric films 14, 16 and 18. Therefore, when each dielectric film 14, 16 and 18 is formed, each connecting hole can be formed and can be filled with metal for connection. Hereby, metal 13 [the contact via under the ferroelectric capacitor] for connecting the lower electrode 19 and the diffused region 5 can be readily formed without forming the connecting hole with extremely large aspect ratio and filling it with metal especially. In addition, as described above, as the number of wiring which is required to be connected to the uppermost wiring layer is not many, high patterning accuracy is not required for the plug for interconnection used for pulling out wiring to the uppermost layer. This is one of the advantages of the present invention obtained by forming buried wiring.

Because Kimura et al. discloses every aspect of claims 41 and 59 except tungsten plugs formed under the ferroelectric capacitors, and goes on to describe the advantages of polysilicon plugs in the claimed multi-layer invention, claims 41 and 59 are

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considered patentable over Kimura et al. either alone or in combination with art that teaches tungsten plugs formed under ferroelectric capacitors.

Response to Arguments

4. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Mon-Thu 8-6.Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Mon-Thu 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TLD 05/2003

Minhloan Tran

Primary Examiner Art Unit 2826